CLAIMS

What is claimed is:

1. A semiconductor device comprising:
   a silicon carbide region having a contact area,
   a substantially uniform and continuous contact region throughout the contact area; and
   a low melting point contact material in direct and substantially continuous contact with the contact region.

2. The semiconductor device of claim 1, wherein the low melting point contact material has a melting point at or below approximately 700 degrees Celsius.

3. The semiconductor device of claim 1, wherein the silicon carbide region comprises p-type silicon carbide.

4. The semiconductor device of claim 1, wherein the contact region comprises an aluminum-silicon carbide alloy.

5. The semiconductor device of claim 1, wherein the contact material comprises substantially pure aluminum.

6. The semiconductor device of claim 1, wherein the contact between the silicon carbide region and the contact material is ohmic.

7. A process for forming an electrical connection to a semiconductor device comprising:
   forming a first metal-containing layer , wherein the first metal-containing layer:
      contacts an exposed region that includes silicon carbide; and
      has a composition that does not form an ohmic contact with a doped silicon carbide if annealed for a time period of less than ten hours and at a temperature less than a melting point of a material within the metal-containing layer; and
   annealing the metal-containing layer and the exposed region, wherein a substantially continuous ohmic contact region is formed between the first metal-containing layer and the silicon carbide.

8. The process of claim 7, wherein the material is aluminum.

9. The process of claim 7, wherein annealing is performed for a time period of at least twenty hours at a temperature in a range of approximately 400-660 C.

10. The process of claim 7, wherein the composition is substantially pure aluminum.

11. The process of claim 7, wherein:
    the material is aluminum; and

the composition comprises aluminum and a first dopant, wherein the composition is at least approximately 90 weight percent aluminum.

12. The process of claim 7, wherein annealing is performed for a time period of at least approximately 25 hours.

13. The process of claim 7, wherein annealing is performed at a temperature no greater than approximately 660 degrees.

14. The process of claim 7, wherein annealing forms an aluminum silicon carbide alloy.

15. The process of claim 7, wherein the exposed region is p-type doped.

16. The process of claim 7, wherein annealing is performed in a vacuum.

17. The process of claim 7, wherein annealing is performed using a noble gas.

18. The process of claim 7, further comprising:
removing a portion of the first metal containing layer; and
forming second metal containing layer over the contact region.

19. A process for forming an electrical connection to a semiconductor device comprising:

    forming a metal-containing layer that contacts an exposed region, wherein the exposed region includes silicon carbide; and

    annealing the metal-containing layer and substrate for a time period of at least approximately ten hours and at a temperature of at least approximately 300 C.

20. The process of claim 19, wherein the metal-containing layer is substantially pure aluminum.

21. The process of claim 19, wherein the metal-containing layer comprises at least approximately 90 weight percent aluminum.

22. The process of claim 19, wherein annealing is performed for a time period of at least approximately 25 hours.

23. The process of claim 19, wherein annealing is performed at a temperature no greater than approximately 660 degrees.

24. The process of claim 19, wherein annealing forms an aluminum silicon carbide alloy.

25. The process of claim 19, wherein the exposed region is p-type doped.

26. The process of claim 19, wherein annealing is performed in a vacuum.

27. The process of claim 19, wherein annealing is performed using a noble gas.

28. The process of claim 19, wherein annealing forms an ohmic contact between the metal-containing layer and the exposed region.